Al2O$_3$/HfO$_2$/p-Si MOS structures : Electrical and structural characterization

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The recent trends in Microelectronic technology concerns the replacement of SiO_2 with high-permittivity (high-k) dielectrics [1-3]. Taking advantage of the higher, compared to SiO_2, permittivity of high-k dielectrics, it is possible to create MOS devices exhibiting simultaneously low Equivalent Oxide Thicknesses (EOT) and low leakage currents. It is found that Al_2O_3 (k~8) is the most promising high-k gate material for future MOS devices, due to the high quality interface that create with the substrates. The main disadvantage of Al_2O_3 is the relative low dielectric permittivity, compared to HfO_2 (k~20) and ZrO_2 (k~20). HfO_2 was the first high-k gate dielectric material introduced, even from the technological node of 45nm, in the MOS technology [4].In this study, we developed structures, using HfO_2 and Al_2O_3 as gate dielectrics. Specifically, 1.5nm HfO_2/p-Si and 2.5nm Al_2O_3/1.5nm HfO_2 /p-Si structures were grown via Atomic Layer Deposition Technique at 250°C. The precursors used for the growth of HfO_2 and Al_2O_3 were Tetrakis(Dymethylamido)Hafnium and Trimethylaluminum respectively. The co-reactant, in both cases, was H_2O. The stoichiometry and the thicknesses of both grown structures as well as the interfaces between Al_2O_3/pGe and HfO_2 /Al_2O_3 were evaluated and characterized through XPS analysis. For the electrical characterization of the developed structures, Al gate electrodes were grown through photolithography and lift of methods. C-V, C-f and J-V measurements were performed and analyzed in order to evaluate the density of interfacial traps (D_{it}), the EOT value as well as to determine the leakage currents through the structures [5].

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